SYSTEM AND METHOD FOR ERROR DETECTION IN ENCODED DIGITAL DATA

Field of the Invention

The present invention relates generally to the field of digital communications. More specifically, the present invention relates to a system and method for providing error detection and/or error correction for digital data.

Background of the Invention

It is common practice to embed into digital data which is to be transmitted an error detection code, such as cyclic redundancy check ("CRC") error detection code, prior to encoding the data. After the data is transmitted and then received, it is common practice to first decode the data and then to compare the error detection code in the received data against expected error detection data. The detection check is performed in order to detect whether errors (error bits) may have resulted from or been introduced along the data's transmission path.

Brief Description of the Drawings

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

Figs. 1 is a block diagram showing portions of a digital data transmitter and receiver according to the prior art;

Figs. 2 is a block diagram showing portions of a digital data transmitter and receiver according to the present invention;

Fig. 3 is a block diagram showing an error detection and correction unit according to the present invention;

Fig. 4 is a flow chart showing the steps of a method of providing error detection and correction according to the present invention.

It will be appreciated that for simplicity and clarity of illustration, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

Unless specifically stated otherwise, as apparent from the following discussions, it is appreciated that throughout the specification discussions utilizing terms such as "processing", "computing", "calculating", "determining", or the like, refer to the action and/or processes of a computer or computing system, or similar electronic computing device, that manipulate and/or transform data represented as physical, such as electronic, quantities within the computing system's registers and/or memories into other data

similarly represented as physical quantities within the computing system's memories, registers or other such information storage, transmission or display devices.

Embodiments of the present invention may include apparatuses for performing the operations herein. This apparatus may be specially constructed for the desired purposes, or it may comprise a general purpose computer selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a computer readable storage medium, such as, but is not limited to, any type of disk including floppy disks, optical disks, CD-ROMs, magnetic-optical disks, read-only memories (ROMs), random access memories (RAMs) electrically programmable read-only memories (EPROMs), electrically erasable and programmable read only memories (EEPROMs), magnetic or optical cards, or any other type of media suitable for storing electronic instructions, and capable of being coupled to a computer system bus.

The processes and displays presented herein are not inherently related to any particular computer or other apparatus. Various general purpose systems may be used with programs in accordance with the teachings herein, or it may prove convenient to construct a more specialized apparatus to perform the desired method. The desired structure for a variety of these systems will appear from the description below. In addition, embodiments of the present invention are not described with reference to any particular programming language. It will be appreciated that a variety of programming languages may be used to implement the teachings of the inventions as described herein.

As part of the present invention there, there may be an error detection unit having a data rate determination unit. The error determination unit may determine a data rate of an encoded block of data received by the error detection. An error checking unit may receive the encoded block of data and an output from the data rate determination unit and in

accordance with the data rate determination unit's output may check the encoded block for a valid codeword. The presence of a valid codeword may indicate that the encoded data is without errors, and the encoded data block may be passed to a de-mapper.

In the event that the error checking unit does not identify a valid codeword in the encoded block of data, a determination may be made regarding the strength of the error correction properties of the error correction code with which the data block was encoded. The strength of the error correction properties of the code may be inversely related to the code's data rate, where the code's data rate may be defined as the inverse of the number of redundant bits produced by the code's algorithm in response to each input source bit. If the code's error correction properties are determined to be strong (e.g. the error correction code used has a low data rate), the encoder block may be passed to a decoder with error correction capability, for example a viterbi decoded. If the code's error correction properties are determined to be weak, the encoded data block may be passed to a second error correction which may correct the encoded data block based on the error detection code within the block.

Turning now to Fig. 1, there is shown a block diagram of a prior art communications system having a data transmitter and receiver. Source bits, which may be produced by any communications application or device, including but not limited to a vocoder or a web browser, may enter the transmitter at point 10. A an error detection code generator 20 (e.g. CRC generator) may generator one or more error detection bits or an error detection codeword which may be appended or inserted to the source bits. The combined source bits and error detection bits may then be encoded by a convolutional encoder 30 or by any functionally equivalent encoder. The encoded data may be separated into block and transmitter after puncturing and interleaving.

In order to regenerate the source bits from a received data signal, a receiver of the prior art first uses a de-interleaver 80, then performs rate matching, decoding, and finally performs an error check to determine whether there are errors in the received signal. In the event that the results of the error check indicate that there are errors in the received signal, it may discard the entire received data block, or may store the received information for further processing.

Turning now to Fig. 2, there is shown a block diagram of a communication system according to the present invention. The transmitter in Fig. 2 is substantially identical to the transmitter in Fig. 1. The receiver, however, has an adapted error detection unit 100 unit which is placed upstream from the decoder 140. The adapted error detection unit is adapted to perform an error check on an encoded signal, rather than on a decoded signal. As part of the adapted error detection unit, there is a rate matcher 102 which may determine the data rate of the encoded block. The data rate information may be used by the error detection unit 104 to identify and validate error detection bits or a codeword within the encoded block of data. Based on the results of the error detection unit 104, the encoded may either be passed to a de-mapper 150, if the encoded block is determined to have no errors, or to a decoder 140 (e.g. viterbi decoder) if error bits are detected in the encoded block.

Turing now to Fig. 3, there is shown an error detection and correction unit according to the present invention having a data rate determination unit 102, an error detection unit 104 and an error correction unit 106. The error correction unit 106 may attempt to correct the error bits within the encoded block based on the error detection code bits or codeword in the block. If, however, the error detection unit 104 determines either that the encoded block has no errors or that the error correction properties of the decoder

140 are sufficiently strong to correct a detected error (e.g. the encoded blocks data rate is very low and thus there is a large number of redundant bits), the error detection unit may pass the encoded data block to the de-mapper 150 or decoder 140.

Turning now to Fig. 4, there is shown a flow diagram with the steps of a method according to the present invention by which an encoded block of data may be checked for errors, may have errors detected and/or corrected, and may be decoded. A encoded data block may be received as part of step 1000, and the block's data rate and/or encoding type may be determined as part of step 2000. Once the data rate and encoding type are determined an error check may be performed as part of step 3000. As part of step 3000, the encoded block may be examined in order to identify error detection bits or an error detection codeword which may have been appended or inserted into the source bits prior to being encoded. The encoded block's data rate may be used as part of step 3000. In one embodiment of the present invention, the encoded block may be examined in only such cases where the block's data rate is 1, and in other embodiments of the present invention, the data rate and encoding type information from step 2000 may be used to perform a mapping function of the encoded block such that the error detection bits or codeword therein may be identified.

Once the error correction bits or codeword are identified, they are checked to determine their validity. Validity may be determined in one of many ways including identifying a pattern in the bits, performing a function on the bits which should produce an expected output, or comparing the received error detection bits with expected error detection bits. Any error code validation method presently known or to be conceived of in the future is applicable to the present invention. If the error detection bits or codeword are determined to be valid, as part of step 4000, the encoded block may be passed to a

de-mapper (step 5000). As part of step 5000, the demapper may de-map the encoded block, thereby producing the encoded block's source bits. If, on the other hand, the error detection bits or codeword are not validated and the data block is determined to have errors, as part of step 6000, a second determination may be made as to the error correction capabilities of the error correction code with which the data block has been encoded. If, for example, the data rate of the encoded block is low and thus the ratio of redundant bits to source bits is high, the encoded block may be passed to a decoded such as a viterbi decoder (step 7000). Once the encoded block is decoded in step 7000, its error detection bits or codeword may be validated as part of step 8000.

Should it be determined, as part of step 6000, that the error correction capabilities of the code with which the data block was encoded is poor, as part of step 9000, the data block may be corrected using its error detection information. That is, an algorithm at least partially using the block's error detection code may attempt to reconstruct the encoded block. In step 10,000, the results of step 9000 are examined to determine whether data block is sufficiently error free to either be de-mapped or decoded (step 11,000). If not, the block may be discarded as part of step 12, 000.

While certain features of the present invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.